Remarks/Arguments

Examiner Victor Yevsikov is thanked for the thorough Office Action.

In the Specification

The specification has been reviewed and amendments made to correct typographical and editorial errors. No new matter has been added.

In the Claims

Claim 1 step c is amended. for support see figures 2 and 3A; Spec p. 7, L 16 to p. 8, L 10.

Dependent claim 8 is a amended. for support see figures 2 and 3A; Spec p. 7, L 16 to p. 8, L 10.

Parent Claim 13 is amended. for support see figures 2 and 3A; Spec p. 7, L 16 to p. 8, L 10.

Dependent claim 17 is a amended. for support see figures 2 and 3A; Spec p. 7, L 16 to p. 8, L 10.

No new matter is added.

In the Drawings

The attached sheet (sheet 4/5) of drawings includes changes to Figure 9 and 10. This sheet 4, which includes Figure 9 and 10 , replaces the original sheet 4 including figure 9 and 10.

The figures are amended as kindly suggested by the examiner. The objection to the drawings figure 9, layer "128" is replaced by layer –144--. For support see spec p. 11, L 2. No new matter is added.

CLAIM REJECTIONS:

Rejection Of Claim 1 Under 35 U.S.C. § 103(a) over Lai (750') In View Of Dirnecker et al. (323')

The rejection of claim 1 under 35 U.S.C. § 103(a) over Lai (750') in view of Dirnecker et al. (323') is acknowledged. Reconsideration and withdrawal of the rejection is respectfully requested in view of the amendments.

Amended Claim 1 states:

> 1. (CURRENTLY AMENDED) A method of fabrication of a capacitor comprising the steps of :
> a) providing a semiconductor structure having a first region and a capacitor region;
> b) forming a first conductive layer over said semiconductor structure;
> c) patterning said first conductive layer to form a plurality of trenches only in said capacitor region and not forming trenches in said first region;
> d) forming a capacitor dielectric layer over said first conductive layer;
> e) forming a top plate over said capacitor dielectric layer in the capacitor region;
> f) patterning said first conductive layer in said first region to form first conductive patterns and a bottom plate;
> g) forming an interlevel dielectric layer over said first conductive layer.

Amended Claim 1's single etch to define conductive lines 104L is non-obvious over Lai's Double etch

Claim 1, step (c) is non-obvious over the combination of references.

In a non-limiting example embodiment shown in figs 2, 3A and 3B, we pattern said first conductive layer 104 to form a plurality of trenches 114 only in said capacitor region and not forming trenches in said first region122.

In contrast, Lai figure 2B, (col. 3. L 26-38) teaches away from claim 1(c), by teaching forming trenches in both the capacitor region and the (frist) region where metal lines are formed. This is a major non-obvious difference. Lai limits the wiring of multilevel interconnect for the rest area to the same metal width and metal line space as that of trench.

The embodiment has many advantages over Lia. In applicant's claim 1, see e.g. figure 3A, trenches 114 are forms only in the capacitor area 122. There is no impact on the first conductive layer in the areas used to make lines. As such, the metal wiring is with full freedom in terms of metal width and metal line space.

Claim 1, step (f) is non-obvious over the combination of references.

In a non-limiting example embodiment shown in figs 7 and 8, we pattern said first conductive layer in said first region to form first conductive patterns (e.g., 104L (e.g., metal lines) and a bottom plate (104B).

In contrast, Lai in figures 2D and 2E, **in a second etch step,** etches the first conductive layer 202 in "the first trenches" to form metal lines. Lai's Double etch to define the metal lines This double etch process deteriorates the process simplicity and manufacturability. In applicant's embodiment, the wiring metal line is not affected by the Capacitor trench process. It is formed at subsequent step when wiring the MIM top electrode, as shown in applicant's figs. 7 and 8.

Claim 1, step g is non-obvious

The combination of reference is improper because there is no motivation to combine the references. The reference solve different problem, have different structures and different incompatible methods. For example, Dirnecker forms a capacitor in a via thru a metal layer in contrast with Lai that forms a capacitor with the metal layer being the bottom plate.

Even if combined, the references do not met the claimed embodiments.

As discussed above, Dirnecker shows a different structure. This combination could only be done with hindsight.

Rejection Of Claims 2- 12 Under 35 U.S.C. § 103(a) over Lai (750') In View Of Dirnecker et al. (323')

The rejection of claims 2-12 under 35 U.S.C. § 103(a) over Lai (750') in view of Dirnecker et al. (323') is acknowledged. Reconsideration and withdrawal of the rejection is respectfully requested in view of the amendments.

The combination of reference is improper because there is no motivation to combine the references. The reference solve different problem, have different structures and different incompatible methods. For example, Dirnecker forms a capacitor in a via thru a metal layer in contrast with Lai that forms a capacitor with the metal layer being the bottom plate.

Even if combined, the references do not met the claimed embodiments.

Claim 6 is non-obvious

Claim 6 states:

6. (ORIGINAL) The method of claim 1 wherein said plurality of trenches formed in a pattern of rows and columns.

Figures 3A and 3B, show an example of claim 6's "said plurality of trenches 114 formed in a pattern of rows and columns". Note that the trenches 114 are formed in the bottom electrode 104C in the capacitor area. See spec. p. 7 , L 16 -19 ; p. 8 L 16 to p. 9, L 4.

The office action on page 4, line 10, posits that Dirnecker figures 28 and 29 show claim 6's arrangement. Dirnecker col. 11, L 41 to 64, and figures 25 & 26 describe figures 28 and 29.

Dirnecker figures 28 and 29 show an non-analogous structure and also show the opposite configuration as claim 6.

First, Dirnecker figures 28 and 29 show an non-analogous structure by showing a metal line 402 that is not part of the capacitor 440 (e.g., (bottom plate) 426 (dielectric) 430 (top plate) 432). See col. 11, L 20 -65. In contrast, Claim 6's trenches 114 are formed in the bottom electrode 104C in the capacitor area. See spec. p. 7 , L 16 -19 .

Second, Dirnecker figures 28 and 29 show the opposite configuration as claim 6. Dirnecker Figure 28 shows via regions 411 that are arranged parallel to each other. In contrast, with claim 6 (figure 3B) that shows the trenches arranged in rows and columns.

Dirnecker Figure 29 shows via regions 411 that are arranged intersect to each other. In contrast, with claim 6 (figure 3B) that shows the trenches arranged in rows and columns. Dirnecker Figure 29 is a "negative or inverse image of" claim 6 (figure 3B). Dirnecker Figure 29 has trenches where applicant's figure 3B has conductive layer.

Amended Claim 8 is non-obvious

Claim 8 states:

> 8. (CURRENTLY AMENDED) The method of claim 1 wherein step (c) further comprises:
> forming a trench resist layer over said first conductive layer; said trench resist layer only has openings that define areas where trenches will be formed in first conductive layer in said capacitor area;
> patterning said first conductive layer to form a plurality of trenches only in said capacitor region;
> removing said trench resist layer.

As discussed above with respect to claim 1 step (c), Lia teaches against claim 8.

Claims 2, 3 4, 6, 8 10 11 and 12 are non-obvious over the cited references.

Claims 2, 3 4, 6, 8 10 11 and 12 are non-obvious over the cited references.

The claims have non-obvious limitations. The claims depend from non-obvious parent claim 1.

Rejection Of Claims 13-14 Under 35 U.S.C. § 103(a) over Lai (750') In View Of Dirnecker et al. (323')

The rejection of claims 13-14 under 35 U.S.C. § 103(a) over Lai (750') in view of Dirnecker et al. (323') is acknowledged. Reconsideration and withdrawal of the rejection is respectfully requested in view of the amendments.

Claim 13 is non-obvious

Claim 13 states.

13. (CURRENTLY AMENDED) A method of fabrication of a capacitor comprising the steps of:
   a) providing a semiconductor structure having a first region and a capacitor region;
   b) forming a first conductive layer over said semiconductor structure;
   c) forming a trench resist layer over said first conductive layer; said trench resist layer has openings that define areas where trenches will be formed in first conductive layer only in said capacitor area; then
   d) patterning said first conductive layer to form a plurality of trenches in only said capacitor region; then

      (1) said trenches extend down into the conductive layer between 24 % and 84 % of the thickness of said first conductive layer;

   e) removing said trench resist layer; then
   f) forming a capacitor dielectric layer over said first conductive layer; then
   g) forming a top plate over said capacitor dielectric layer in the capacitor region; said top plate is formed by forming a top plate layer over said capacitor dielectric layer; and masking and patterning said top plate layer; then
   h) patterning said first conductive layer in said first region to form first conductive patterns and a bottom plate; said first conductive patterns comprise a n-l level metal layer;
   i) forming an interlevel dielectric layer over said first conductive layer and said top plate;
   j) forming via contacts in said interlevel dielectric layer to contact said top plate, said bottom plate and said first conductive patterns;
   k) forming second conductive layer contacting said via contacts; said second conductive layer is a n level metal layer.

Claim 13 steps (c) (d) and (h) are non-obvious over the cited references for the reasons stated above with respect to claim 1.

Therefore Claim 13 is submitted to be allowable over the cited references and reconsideration and allowance are respectfully solicited.

Rejection Of Claims 15-17 Under 35 U.S.C. § 103(a) over Lai (750') In View Of Dirnecker et al. (323')

The rejection of claims 15-17 under 35 U.S.C. § 103(a) over Lai (750') in view of Dirnecker et al. (323') is acknowledged. Reconsideration and withdrawal of the rejection is respectfully requested in view of the amendments.

Claims 15 to 17 have non-obvious limitations and depend from non-obvious parent claims.

DRAWING OBJECTION

The objection to the drawings is acknowledged. Reconsideration and withdrawal of the rejection is respectfully requested in view of the amendments. The attached sheet (sheet 4/5) of drawings includes changes to Figure 9 and 10. This sheet 4, which includes Figure 9 and 10 , replaces the original sheet 4 including figure 9 and 10. The figures are amended as kindly suggested by the examiner. The objection to the drawings figure 9, layer "128" is replaced by layer –144--. In addition, element number --144— was added to figure 10. For support see spec p. 11, L 2. No new matter is added.

CONCLUSION

In conclusion, reconsideration and withdrawal of the rejections are respectfully requested. Allowance of all claims is requested. Issuance of the application is requested.

It is requested that the Examiner telephone the undersigned attorney at (215) 670-2455 should there be anyway that we could help to place this Application in condition for Allowance.

Respectfully submitted,

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